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REMARKS

Claims 20-27 stand rejected under 35 U.S.C. § 103 as being unpatentable over JP '339 in view of Akiyama '558 ("Akiyama"). Claim 20 is independent. This rejection is respectfully traversed for the following reasons.

The Examiner admits that JP '339 does not disclose a first upper wire that is electrically connected with a top surface of an upper electrode. The Examiner therefore alleges that Akiyama "teaches a mim capacitor in which an upper wire 20 that is electrically connected to the lower wire 14a is formed on an upper electrode 16 of the capacitor [(Fig. 4)]" whereby it would have been obvious to modify JP '339 with the teachings of Akiyama "*to overcome problems as recited in [0009], [0010], and [0011] of Akiyama.*"

It is respectfully submitted that the proposed modification is improper because the Examiner has not provided the requisite ***objective*** evidence ***from the prior art*** that "suggests the desirability" of the proposed modification. As is well known in patent law, a *prima facie* showing of obviousness can only be established if the prior art "suggests the desirability" of the proposed modification using objective evidence.

In the instant case, it is respectfully submitted that the Examiner's relied on "objective" evidence for adding the upper wire 20 of Akiyama onto the alleged upper electrode 168 of JP '339 is in fact, completely unrelated to the proposed modification. Specifically, the Examiner alleges that Akiyama suggests the desirability of providing an upper wire on an upper electrode "to overcome problems as recited in [0009], [0010], [0011] of Akiyama." However, Akiyama does not disclose or suggest that the problems discussed in [0009], [0010], [0011] of Akiyama are overcome by using the upper wire/upper electrode arrangement relied on by the Examiner to modify JP '339.

As described in [0009], [0010], [0011], the problems which Akiyama attempts to overcome are related to the capacitor being formed to project from the surface of the dielectric film 2 on Si substrate 1 (*see* Fig. 15 of Akiyama) and the contact portions 8a-8b associated with the upper-level wiring lead 9 being different in depth from each other (*see* Fig. 16 of Akiyama). To obviate these issues, Akiyama expressly discloses in [0043] that because:

> the ***capacitor and the wiring leads are planarly buried in the grooves***, the ILD film 17 shown in FIG. 4 does no longer call for any planarization processing. Thus, the planarization steps required in the process decreases in number as compared to the prior art discussed in the introductory part of the description. Furthermore ***the capacitor of this embodiment is not projected from the dielectric film 12***. Resulting in the contact holes 19a-19b of FIG. 4 becoming the same in depth as each other, the contact holes are definable without suffering from any risks of over-etching damages

Accordingly, Akiyama, at best, provides motivation for planarly burying a capacitor and wiring leads in a groove so that the capacitor is not projected from the dielectric film. Akiyama does NOT provide any motivation or rationale for providing an upper wire on an upper electrode. In fact, as shown in Figure 16, Akiyama's admitted prior art already shows an upper wire provided on an upper electrode, thereby evidencing that Akiyama's objective of obviating the problems discussed in [0009], [0010], [0011] is not based on, nor related to, forming an upper wire on an upper electrode. It is therefore respectfully submitted that Akiyama does not provide any motivation or rationale for providing an upper wire on the alleged upper electrode of JP '339. Without any disclosed need or desire from the prior art for providing an upper wire on an upper electrode, it is respectfully submitted that the proposed modification lacks the requisite motivation required under § 103 for establishing obviousness.

Indeed, it is respectfully submitted that one of ordinary skill in the art would not make the proposed modification because it would unnecessarily increase the number of processes, time

and cost associated with manufacturing a semiconductor device. The Examiner is directed to the attached exhibit which illustrates the sequence by which the attempted modification by the Examiner would take place. As shown in Fig. (a), region B of the second capacitor electrode 168 is electrically connected to the lower wire 320 through region A of the second capacitor electrode 168. If a third conductive film were to be formed on the second capacitor electrode 168, region A of the second capacitor electrode 168 would need to be removed (*see* Fig. (b)) and an insulating film 2 would need to be formed on and around the region B of the second capacitor electrode 168. Then, the insulating film 2 would need to be etched away to form the space for the third conductive film 1 (*see* Fig. (c)). Accordingly, the proposed modification would, as discussed above, unnecessarily increase the number of processes, time and cost associated with manufacturing a semiconductor device.

In contrast, as discussed throughout Applicants' specification, one of the objects of the present invention is directed to reducing processing steps, which can be enabled by the novel combination of elements recited in the particular arrangement set forth in claim 20 (discussed generally on page 2, lines 22-24 and specifically throughout Applicants' specification). Only Applicants have recognized such a problem in, for example, MIM capacitors, and conceived of the novel structural combination of elements which can enable obviating such a problem. In this regard, it is respectfully submitted that none of the cited prior art discloses or suggests the ***combination*** of elements arranged in the particular manner set forth in claim 20. At best, the Examiner has attempted to show only that the elements of the claimed invention are ***individually*** known without providing a *prima facie* showing of obviousness that the ***combination*** of elements recited in the claims is known or suggested in the art. For all the foregoing reasons, it is respectfully submitted that the proposed combination of JP '339 and Akiyama is improper.

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The Examiner is directed to MPEP § 2143.03 under the subsection entitled "Fact that References Can Be Combined or Modified is Not Sufficient to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (*In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990)).

In the instant case, even assuming *arguendo* that JP '339 can be modified by Akiyama, it is submitted that the "mere fact that [JP '339 and Akiyama] can be combined ... does not render the resultant combination obvious" because nowhere does the ***prior art*** "suggest the desirability of the combination" as set forth by the Examiner. Again, there is no ***disclosed*** need or desire, absent Applicants' specification, for providing an upper wiring on the alleged upper electrode 168 of JP '339.

The Examiner is further directed to MPEP § 2143.01 under the subsection entitled "Fact that the Claimed Invention is Within the Capabilities of One of Ordinary Skill in the Art is Not Sufficient by Itself to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> A statement that modifications of the prior art to meet the claimed invention would have been [obvious] because the references relied upon teach that all aspects of the claimed invention were ***individually*** known in the art is ***not*** sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. (citing *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)).

In the instant case, even assuming *arguendo* that JP '339 and Akiyama "teach that all aspects of the claimed invention [are] individually known in the art", it is submitted that such a conclusion "is not sufficient to establish a *prima facie* case of obviousness" because there is no ***objective*** reason on the record to combine the teachings of the cited prior art. Indeed, Akiyama is silent as to suggesting the desirability of the upper wiring structure 20 for any particular reason, and

instead merely emulates Akiyama's admitted prior art shown in Figure 16 thereof in relation to the upper wiring structure 20. As previously mentioned, Akiyama is directed to forming the capacitor within the insulating layer 12 (*see* Figure 4), *independent of the existence of the upper wiring structure 20*, in an attempt to avoid the issues raised in [0009], [0010], [0011].

Moreover, it is respectfully submitted that patentable subject matter typically arises from using ***known*** elements/processes in novel ***combinations***. Accordingly, the Examiner's allegations that the elements recited in the pending claims are well-known separately is irrelevant to the determination of patentability for the ***combination*** thereof. In this regard, it is noted that the Examiner rejects many of the dependent claims by simply alleging that the claimed features are well-known generally. However, such a conclusion is not sufficient to establish obviousness under the requisites of § 103 because, in the instant case, the Examiner has neither shown prior art to support his claim nor provided any motivation from the prior art to support the position that using the alleged well-known elements in the specific combination set forth in claim 20 would have been obvious.

The Examiner has apparently relied on Official Notice. Pursuant to MPEP § 2144.03(C), Applicant hereby challenges the Examiner's "well-known" allegations set forth in the Office Action (including many dependent claims). If the pending rejections are maintained, Applicants respectfully request documentary evidence of the Examiner's findings, along with motivation from the prior art for modifying JP '339 by incorporating the allegedly well-known elements in *the particular manner set forth in claim 20*.

In view of the foregoing, it is respectfully submitted that none of the cited prior art, alone or in combination, discloses or suggests the novel ***combination*** of elements recited in claim 20. Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon

which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 20 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination. Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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